



T1 OVERVIEW
THE HIGH-CAPACITY
DIGITAL NETWORK

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THE HIGH-CAPACITY DIGITAL NETWORK

High-Capacity, Digital Signal Level 1 (DS1 Hi-Cap) service, also known as T1, is just one type of Hi-Cap service available to telephony customers. There is a higher order, or hierarchy, of T1 such as DS2, also known as T2, or DS3, also known as T3, that also may be ordered. However, the focus of this document is on T1 service.

T1 is a high speed network developed by AT&T in 1957 and implemented in the early 1960s. The technology was developed to support long-haul pulse-code modulation (PCM) voice transmission. The innovation of T1 was to introduce digitized voice and to create a communication link that enables transmission of voice, data and video signals at the rate of 1.544 million bits per second (Mb/s). The telephone companies initially used T1 to reduce the number of telephone cables in a large metropolitan area. A DS1 Hi-Cap, or T1, is:

- A point-to-point service.
- 1.544 Mbps digital pipe —Transport Technology

The T1 may be provided using fiber optic transport devices or copper cable facilities.

T1 Service

Due to installation costs, early T1 services were used primarily by phone companies and the federal government. Customers, particularly those not requiring all of the bandwidth available on a T1 circuit, would have needed to purchase expensive multiplexing equipment not required for analog transmission. The cost of multiplexing equipment, plus the fact that service charges were still based on the amount of bandwidth purchased, did not make T1 an economic decision for many potential customers. T1 was re-tariffed in the early 1980s to allow substantial cost savings to customers who had multiple circuits between two locations. With customer requirements for interlocation connectivity, growth rates have continued to climb for services such as:

- Internet Service Provider (ISP) access
- ISDN Primary Rate Interface (ISDN PRI) access
- Channel Service for multiple applications
- Local Area Network/Wide Area Network (LAN/WAN) connectivity for data transfer and sharing
- Medical data transfer (i.e., X ray, CAT scan)
- Mainframe computer links
- Videoconferencing
- Private Branch Exchange (PBX) connectivity

- Connect cellular sites
- Interexchange Carrier (IC)

Note: The PRI circuit requires special dial-through testing not associated with a point-to-point T1.

Customer Benefits

Some of the drivers behind the demand for T1 service are:

- Flexibility
 - T1 handles voice and/or data services.
 - Bandwidth can be allocated on demand.
- Improved quality over analog lines.
- Increased capacity over conventional lines:
 - 1-24 standard voice/data channels (DS0s).
- Guaranteed Service
 - Most carriers strive to offer restoration in less than 3 hrs.
 - Available 99.99 percent annually.

In the past decade, costs have been reduced from tens of thousands of dollars per month to around \$500 per month and installation times (customer due dates) have gone from several weeks to same-day service.

Technology Review

A vast majority of T1 benefits are attributed to the fact that voice and data share a single digital communication link. Computer data consists of 1's and 0's, the symbols of the binary system; therefore computer data is already compatible with T1's digital format. Voice presents another challenge. Voice signals actually comprise of complex analog waveforms.

Sine waves are all we have to work with in transmitting over the analog telephone channel because it doesn't transmit pulses. Digital transmission systems will transmit pulses, and with them we can encode either analog or digital information by modulating pulses. There are a few ways to modulate a series of pulses to carry data.

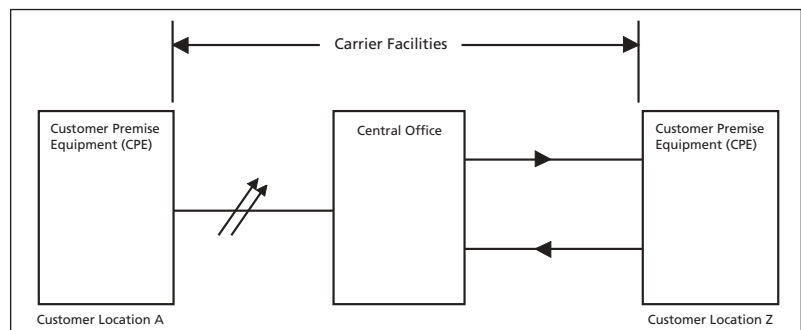


Figure 1: DS1 Hi-Cap, T1

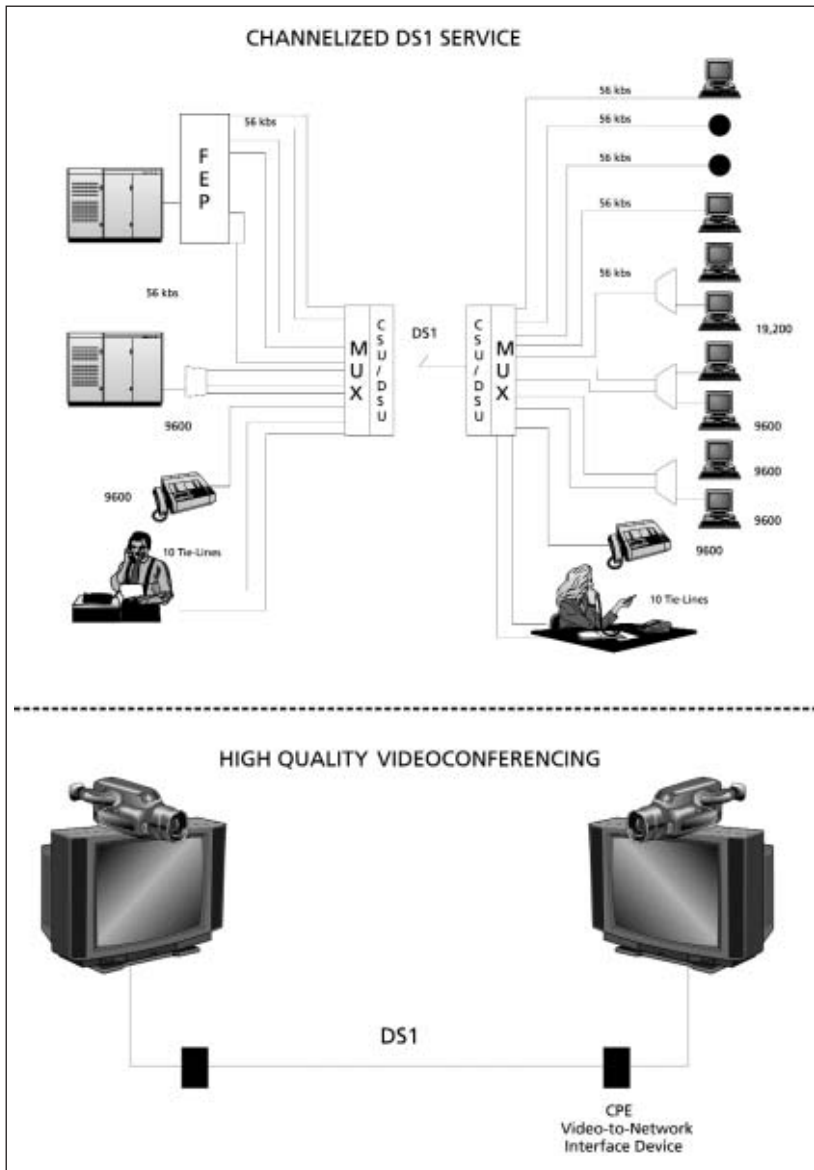


Figure 2: DS1 Service

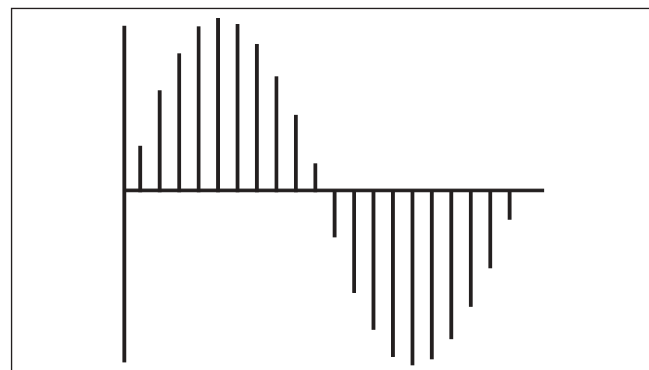


Figure 3: Pulse Amplitude Modulation (PAM)

When the amplitude of the pulses is varied to represent analog information, the method is called pulse amplitude modulation (PAM). This method is very susceptible to electrical noise interference.

The process of sampling an analog signal as in Pulse Amplitude Modulation, but where the amplitudes of the samples are encoded into binary numbers represented by constant amplitude pulses is called Pulse Code Modulation (PCM). This method overcomes the noise interference problem of Pulse Amplitude Modulation. The PCM system used by communication carriers employs a three step process: sampling, quantization and coding. During the sampling process, the analog signal is sampled 8,000 times per second.

The resulting samples represent an infinite number of voltages. Thus, the second step in the PCM process, called quantization, reduces the PAM signal to a limited number of discrete amplitudes. The third step in the PCM process, known as coding, reduces the number of unique values of the PAM signal so they can be coded through the use of an 8-bit byte. For simplicity, the lower portion of the diagram in Figure 4 uses 4 bits to represent each PAM signal; however, in actuality 8 bits are used. The 8,000 samples per second multiplied by the 8 bits per sample create the 64 kb/s rate known as Digital Signal Level Zero (DS0).

Once digitized, voice and/or data signals from various sources can be combined, or multiplexed, and transmitted over a single T1 link. This process is known as Time Division Multiplexing (TDM).

TDM divides a T1 link into 24 discrete 64 kb/s time slots. An identical number of DS0 signals, representing 24 separate voice and/or data calls, are assigned to each time slot for transmission within the link. PCM and TDM are keys to understanding the basic T1 rate of 1.544 Mb/s.

In T1, the 8 bit digital samples created in the PCM step, for voice traffic only, are grouped into the 24 discrete DS0 time slots created by TDM. Each group of 24 time slots is referred to as a T1 Frame. Since there are 24 time slots, each containing 8 bits, the number of bits per frame totals 192. To mark the end of one frame and the beginning of another frame, a 193rd bit is added. This additional bit is called the framing bit. Since DS0 signals are sampled 8,000 times per second, it means that 8,000 192-bit information frames are

created during that period. 8,000 samples per second multiplied by 192 bits totals 1.536 Mb/s. At 8,000 samples per second, framing bits are created at the rate of 8 kb/s. The result is a single 1.544 Mb/s signal known as digital signal level one (DS1).

The DS1 signal starts strong when it is newly created, but degrades rapidly as it travels along the transmission media. Factors such as attenuation and dispersion attribute to signal degradation. To compensate for signal loss, regeneration repeaters are used to sample and recreate the original signal at periodic intervals along the T1 link.

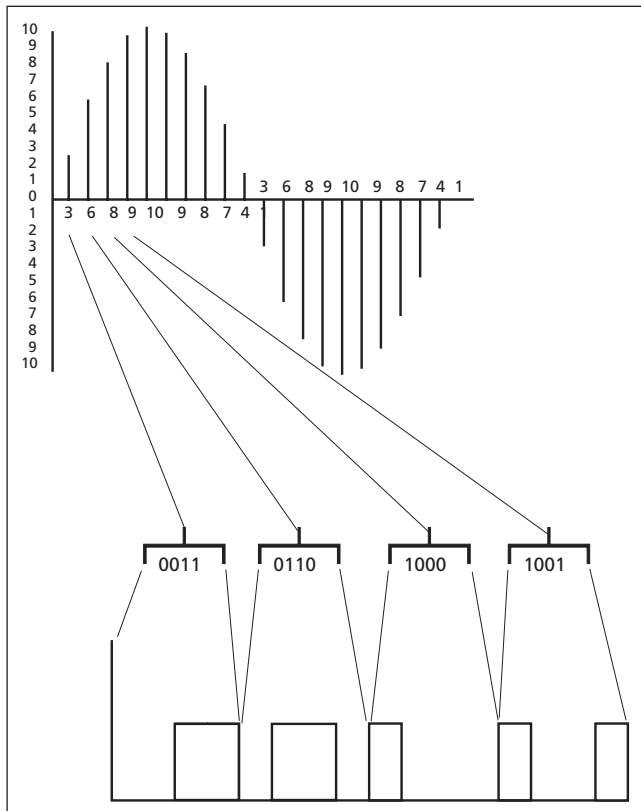


Figure 4: Pulse Code Modulation

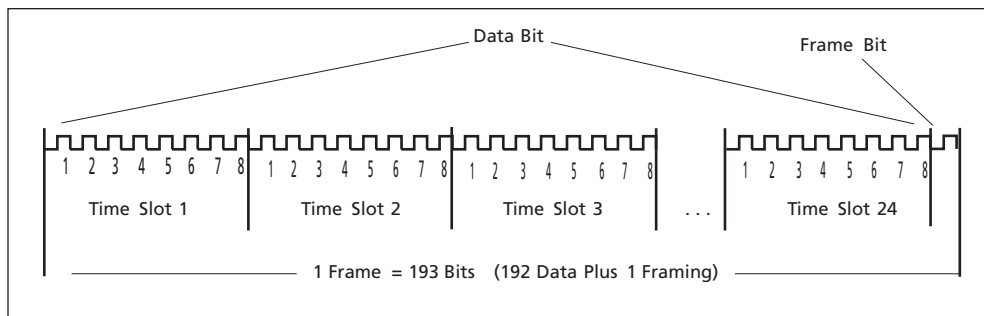


Figure 5: Typical T1 Frame Created through TDM

Since the signal consists of 1's and 0's, recreating it is not a complicated task. Repeaters are typically at 6000-foot intervals for copper lines.

A DS1 signal is transmitted on the T1 link in a binary format of 1's and 0's. Regeneration repeaters rely on proper DS1 format to recognize the DS-1 signal and distinguish it from line noise. Alternate Mark Inversion (AMI) is a very common format that is used over metallic transmission media.

In the AMI signaling format, the binary value of 1 is represented by a square wave (pulse); the binary value of 0 is represented by a straight line (no pulse). A bipolar format is used to achieve superior signal travel distance and to offer a built-in method for error detection. If consecutive pulses of the same polarity are detected a bipolar violation (BPV) will be created. BPV's indicate that the signal input has been disturbed due to environmental conditions or defective equipment.

Regeneration repeaters must know when to sample the bipolar signal to determine whether a 0 or a 1 is being transmitted at any given time. To ensure proper sampling, the repeater relies on a timing method that uses the binary pulses (ones) to maintain synchronization with the network equipment that is transmitting the DS1 signal.

Pulses are critical for maintaining proper signal timing, therefore, DS1 signals are required to meet specific ones density standards. The standards require that at least one pulse be transmitted within any eight-bit sequence. Since long strings of consecutive zeros between digital values have devastating effects on timing, ones density standards prohibit the transmission of more than 15 zeros in succession.

Meeting ones density requirements can vary depending on the application. The size and content of the bit patterns representing human speech are constant, therefore, with voice applications acceptable ones density is virtually guaranteed. In data applications, however, the computer data is highly variable in size and content. Conformance to ones density cannot always be guaranteed. Bipolar with 8-Zero

Substitution (B8ZS) is a technique that addresses this problem.

B8ZS uses intentional BPV's in the data stream to break up long strings of zeros. With B8ZS coding, each block of 8 consecutive zeros is replaced with the B8ZS code word. The BPV's are placed in bit positions 4 and 7. Bit positions 5 and 8 are also

substituted with pulses that alternate the pulses used in bits 4 and 7. This is the standard for "Clear Channel Capability." AT&T references it in Publication 62411 in Appendix B as CB144. It is also part of the ANSI T1.403-1989 standard.

Individual bits in the 1.544 Mb/s DS1 signal have no meaning unless they are organized in an orderly and understandable manner. Framing allows proper channel alignment for encoding and decoding each channel's eight bit word. As framing bits are received, they are saved to form a pattern, which is checked by T1 equipment. When the proper pattern is detected, the state of frame synchronization (frame sync) occurs.

The three predominate framing formats are D4 (Super Frame), Extended Super Frame, and Lucent Technologies' Subscriber Line Carrier (SLC), as described in Table 1.

The D4 framing pattern, shown in Table 2, consists of two interleaved patterns. The terminal framing pattern (ft) marks super frame boundaries so that receiving equipment can correctly process the customer's voice or data information. The terminal framing pattern is a repeating ones and zeros in odd numbered frames. The signaling frame (fs) is a pattern of "001110" placed in the even numbered frames. Notice that frames with signaling information are marked by changes in the bit pattern. Control bits 2 and 4 contain zeros; control bit 6 is coded as a one. This indicates that the sixth frame contains signaling information. Control bits 8 and 10 contain ones, control bit 12 is coded as a zero, and thus indicating the 12th frame contains signaling information.

A process known as robbed bit signaling is used to enable the sharing of signaling bits by all 12 frames in the super frame. Robbed bit signaling uses the least significant bit (8th) of the DS0's in frames 6 and 12 for signaling information. The steady state of the bit, 0 or 1, indicates whether the called device is on-hook, off-hook, disconnected, busy, etc.

The need to test a system's performance without disrupting service fueled the development of the Extended Super Frame format (ESF), outlined in Table 3. With ESF the super frame is extended from 12 to 24 DS1 frames. The 193rd bit (just like the D4 format) in each frame is used as a control bit. ESF uses three-fourths of its 24 control bits for evaluation of circuit performance. Six control bits are used for a Cyclic Redundancy Check (CRC). CRC is a method of detecting errors as information is transmitted along the T1 link. Twelve control bits are used as a data link for communication between transmitting and receiving equipment at either side of the T1 link; and another six bits are used to manage signaling and framing.

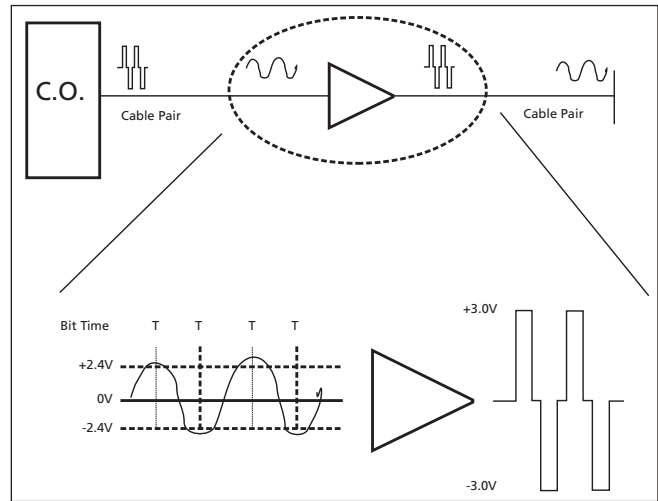


Figure 6: Regenerative Repeaters

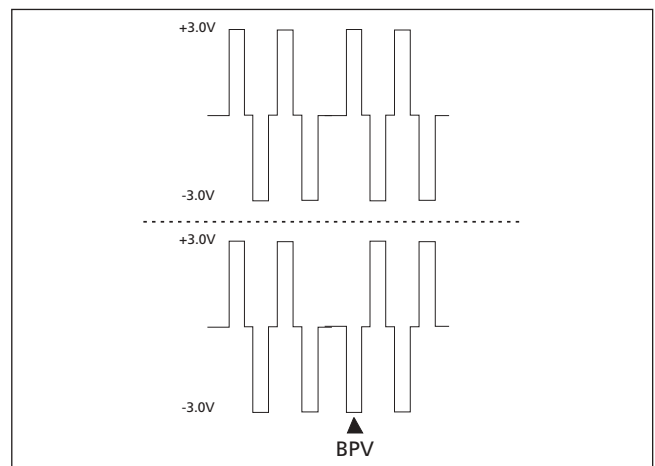


Figure 7: AMI and AMI with bipolar violation

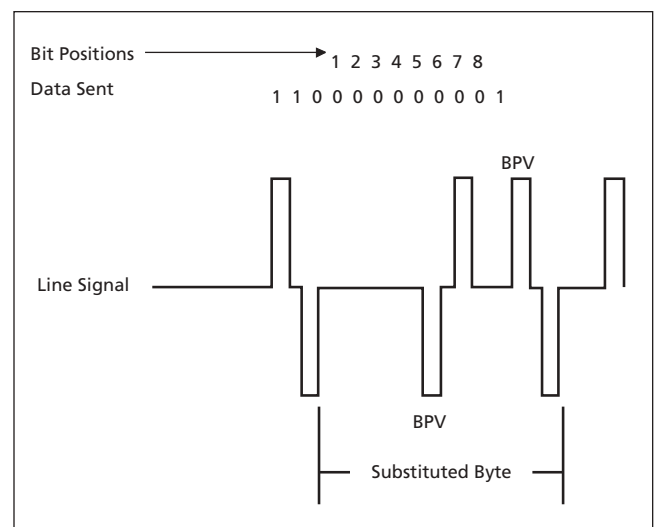


Figure 8: Bipolar with 8-Zero Substitution

CRC-6 is a six-bit word that detects bit errors in any block of live data. First, the network equipment building the ESF performs a mathematical calculation on the signal to be transmitted across the T1 link. Control bits are not used in this calculation. Second, the signal is transmitted across the T1 link to the receiving equipment. The result of the mathematical calculation is a six bit word which is sent to the

receiving equipment in the six CRC bit positions of the next consecutive ESF. Third, the receiving network equipment performs the same mathematical calculation on the customer information, and compares the result with the six bit word which arrives in the next consecutive ESF. If results match, no bit errors have occurred; if results do not match one or more logic errors have occurred.

Table 1: Frame Formats

Frame Formats	Description
D4, Super Frame	D4 is the standard framing used for channel banks. It consists of 12 consecutive DS1 frames. Framing bits are used for synchronization and to indicate the robbed-bit signaling frames.
Extended Super Frame (ESF)	ESF is 24 consecutive DS1 frames where the framing bits are used for more than just synchronization. One of the key benefits of ESF is that it provides a Cyclic Redundancy Check (CRC), an advanced means of in-service error checking for the signal. CRC errors mean the customer is receiving incorrect data. In addition, ESF provides 12 Facility Data Link (FDL) bits that the customer can use for performance monitoring and a variety of other purposes.
SLC	SLC framing alters the framing bits to allow communication between the remote terminal and the Central Office terminal.
Unframed	This non-standard signal format provides a full 1.544 Mbps for customer data, with no framing bits added for synchronization timing. It is used for point-to-point circuits only, where no clocking or synchronization from the network is required. A DS1 analyzer test set will indicate a good T1 signal without frame sync. Note: An unframed ALL ONES signal is sometimes used to test repeater spacing. It allows a true 772 kHz signal.

Table 2: D4 (Super Frame) Framing

Frame No.	Terminal Framing	Signal Framing	Information Bits	Signaling Bits	Signaling Frame
1	1	—	1-8	—	
2	—	0	1-8	—	
3	0	—	1-8	—	
4	—	0	1-8	—	
5	1	—	1-8	—	
6	—	1	1-7	8	A
7	0	—	1-8	—	
8	—	1	1-8	—	
9	1	—	1-8	—	
10	—	1	1-8	—	
11	0	—	1-8	—	
12	—	0	1-7	8	B

Twelve control bits in ESF are used as a data link for communication between transmitting and receiving equipment at either side of the T1 link. These 12 control bits can be used for any purpose. A typical application is to use them for trouble flags. The yellow alarm signal is an example of a trouble flag that can be transmitted in the ESF data link. If synchronization to a transmitted DS1 signal cannot be achieved, a yellow alarm will be sent.

In addition to enhanced circuit management, ESF provides enhanced signaling capability. Robbing the 8th bit from the 6th, 12th, 18th, and 24th frames in the super frame, more than 16 signaling states can be represented. Enhanced signaling compliments services such as video.

The SLC-96, shown in Figure 9, is an outside plant system that uses four T1 lines, converts them to 96 DS0 lines, and feeds them to individual customers. The framing bits have been altered. When testing, the correct framing format must be selected to be compatible with this system.

In SLC-96 framing the frame terminal (ft) bits provide the framing format. The ft bits are configured the same as for D4 framing. The frame signaling (fs) bits have been altered to provide alarming, switching and concentration. The modified frame terminal and signaling bits provide a special Data Link A, over span A.

Table 3: Extended Super Frame (ESF)

Frame No.	SYNC	CRC	Data Link	Information Bits	Channel Signal	
1	—	—	—	X	1-8	
2	—	—	C1	—	1-8	
3	—	—	—	X	1-8	
4	0	—	—	—	1-8	
5	—	—	—	X	1-8	
6	—	—	C2	—	1-7	A
7	—	—	—	X	1-8	
8	0	—	—	—	1-8	
9	—	—	—	X	1-8	
10	—	—	C3	—	1-8	
11	—	—	—	X	1-8	
12	1	—	—	—	1-7	B
13	—	—	—	X	1-8	
14	—	—	C4	—	1-8	
15	—	—	—	X	1-8	
16	0	—	—	—	1-8	
17	—	—	—	X	1-8	
18	—	—	C5	—	1-7	C
19	—	—	—	X	1-8	
20	1	—	—	—	1-8	
21	—	—	—	X	1-8	
22	—	—	C6	—	1-8	
23	—	—	—	X	1-8	
24	1	—	—	—	1-7	D

T1 Architecture

The Digital Signal, Level 1 (DS1) at 1.544 Mbps is the fundamental building block for communications transport, both voice and data. It is sometimes viewed as the primary telephone company (telco) bypass vehicle. In 1996, Interexchange Carriers (ICs) accounted for nearly 81 percent of a telco's T1 service.

There are several methods and equipment types available for providing T1 transport to the local customer. The most common methods are:

- Local copper cable (four-wire) with T1 repeaters, known as a standard repeatered T1 Span.
- Local copper facilities (four-wire or two-wire) using High-Bit-Rate Digital Subscriber Line (HDSL) technology (a.k.a. Express Band) for non-repeatered and repeatered HDSL.
- Over local fiber facilities such as:
 - Fiber Optic Terminal (FOT) equipment at the customer's premises.
 - Fiber facilities to a local Next Generation Digital Loop Carrier (NGDLC) with a local copper feed to the customer.

A local T1 circuit may cross-connect to a variety of equipment or transport facilities at the Central Office (C.O.), such as:

- A digital switch T1 interface port
- An FOT for pass-through access to an Interexchange Carrier (IC)
- A C.O. channel bank (multiplexer)
- Another local T1 circuit for end-to-end T1 for a local customer

The overall circuit layout of a typical DS1 Hi-Cap is a point-to-point circuit from customer Location A to customer Location Z, consisting of:

- A Customer Service Unit (CSU) and other multiplexing or terminal equipment.
- Interexchange network or Interoffice Facility (IOF) equipment such as:
 - A Digital Cross-Connect System for T3 to T1 connection (DCS or DACS)
 - Fiber Optic Terminal (FOT), usually SONET compatible, or a digital microwave radio serving as the Interexchange Carrier Point of Interface (IC-POI)

■ Local Serving Office (LSO) telco equipment such as:

- An RJ48, which serves as the End-User Point of Termination (EU-POT)
- A Network Interface Unit (NIU) or Smart Jack
- Local span facilities (either copper or fiber)
- A central office Main Distribution Frame (MDF)
- An Office-Terminating Repeater (OTR)
- A Digital Signal Cross-Connect (DSX)
- An OTR or multiplex equipment to/from the far-end location, which may be identical to near-end equipment

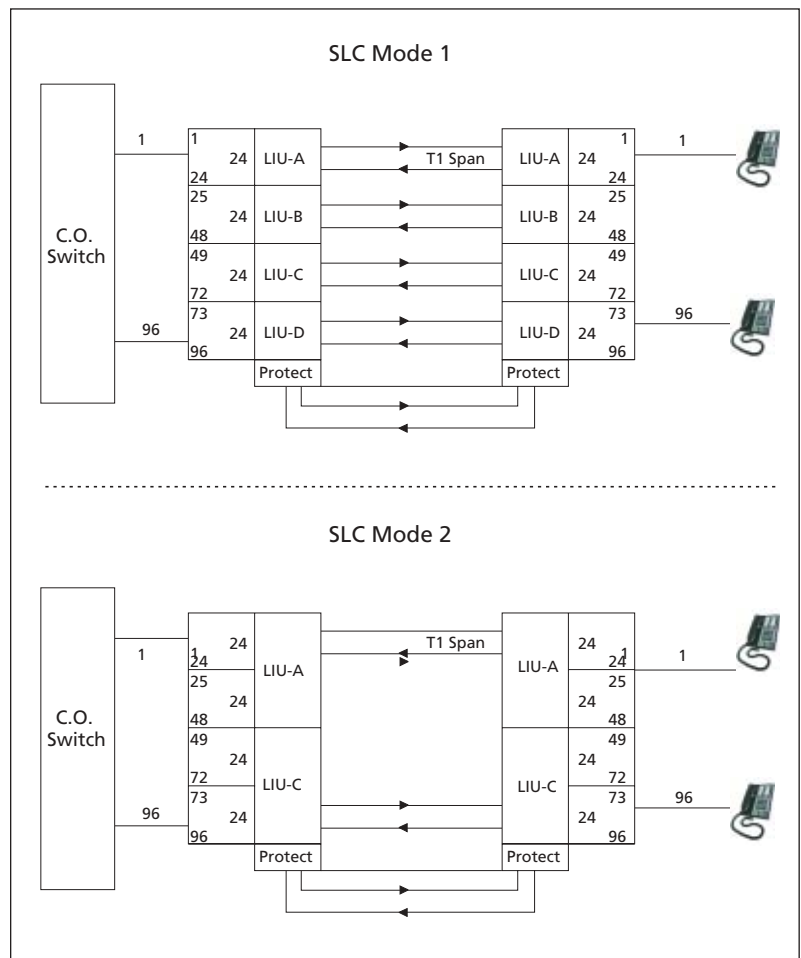


Figure 9: The SLC-96 System—Mode 1 and 2

T1 Equipment Function

Customer Service Unit (CSU)

The Customer Service Unit is located at the customer's premises and is considered Customer Premise Equipment (CPE). A CSU interfaces the network facility to the CPE, but is not required on all circuits. Signal format is determined by the CSU along with timing recovery for synchronization. Monitoring the receive signal to check for errors (CRC-6) and monitoring the transmit signal for proper ones density are responsibilities of the CSU. In the event of CPE failure, the CSU transmits a blue alarm, or keep-alive signal (all ones). During testing of the T1 circuit, the CSU can be placed into a loopback mode.

Demarcation Point

The demarcation point, also referred to as the Demarc, DMARC, or DP, at the End-User Point of Termination (EU-POT) is typically defined as one of the following jacks:

- RJ48C for a single circuit
- RJ48H for up to 12 circuits
- RJ48M for up to eight circuits
- RJ48X for a single circuit, with network shorting bars

The RJ48X, the most commonly recommended jack, is useful for loop extensions. Its network shorting bars provide a loopback if the CSU is removed. The RJ48H and RJ48M jacks are used mostly with Digital Data Services (DDS).

The Demarcation jack will typically be clearly labeled with circuit identification code and the current signal level. The Federal Communications Commission (FCC) states that the Demarc (NIU) should be within 12 inches of the protection or building terminal. The Demarc should never extend past the NIU. The Inside Wire (IW) extending the loopback device into the building is considered customer premise equipment (CPE).

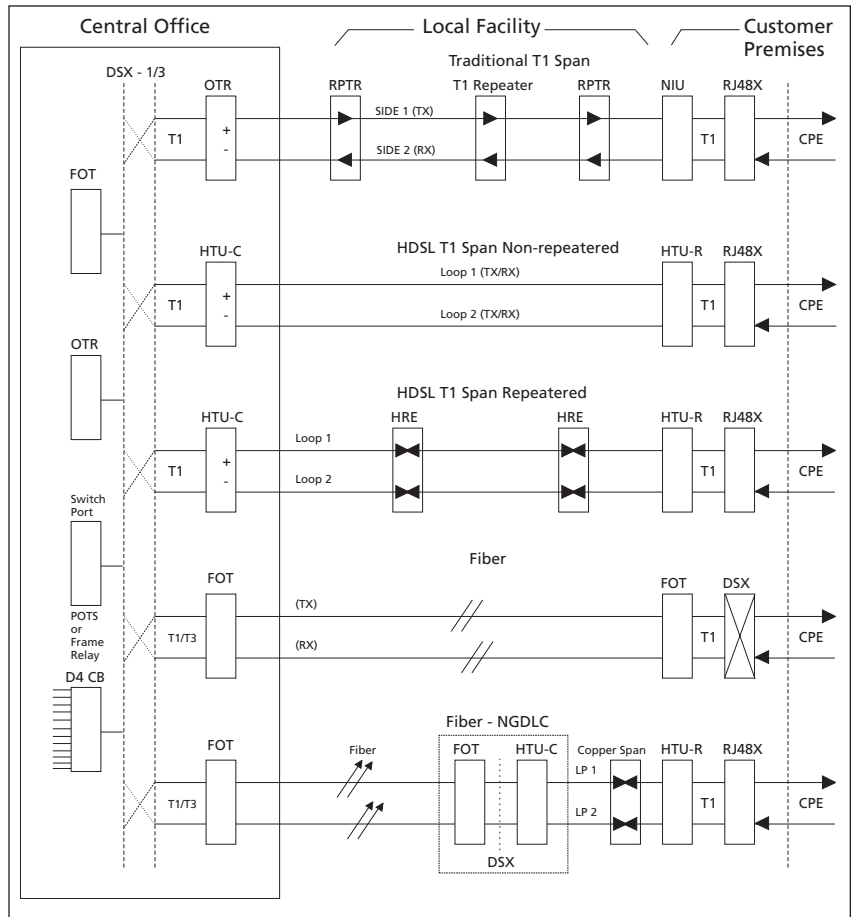


Figure 10: DS1 Hi-Cap Architecture

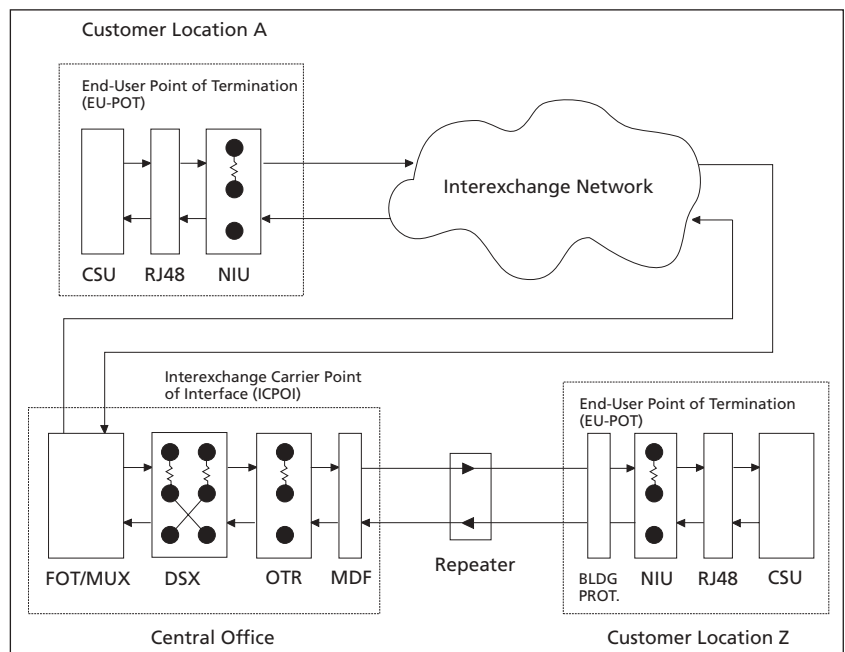


Figure 11: Circuit Layout

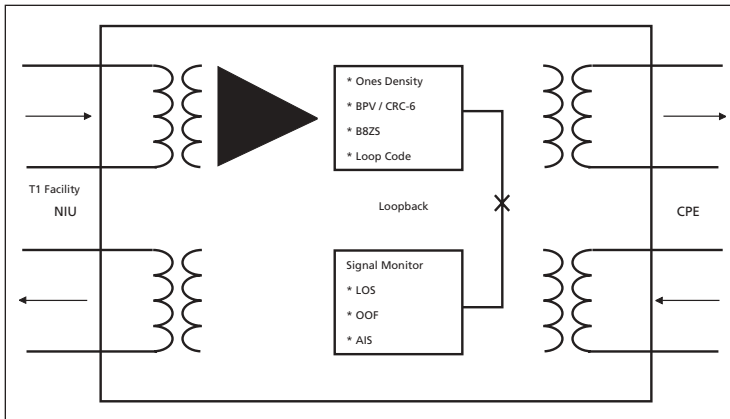


Figure 12: Customer Service Unit (CSU)

Network Interface Device (NID)

The Network Interface Device (NID) is provided and maintained by the Service Carrier and acts as the termination point of the Service Carrier’s network. The NID is a FCC Part 68 Registered Jack from which the Inside Wire (IW) may be disconnected from the regulated Service Carrier network.

Station Wire Color Code

Service Providers typically use two basic types of station wire: two-pair or three-pair. The two-pair and three-pair station wire also comes with one of two possible color codes as shown in the Table 4.

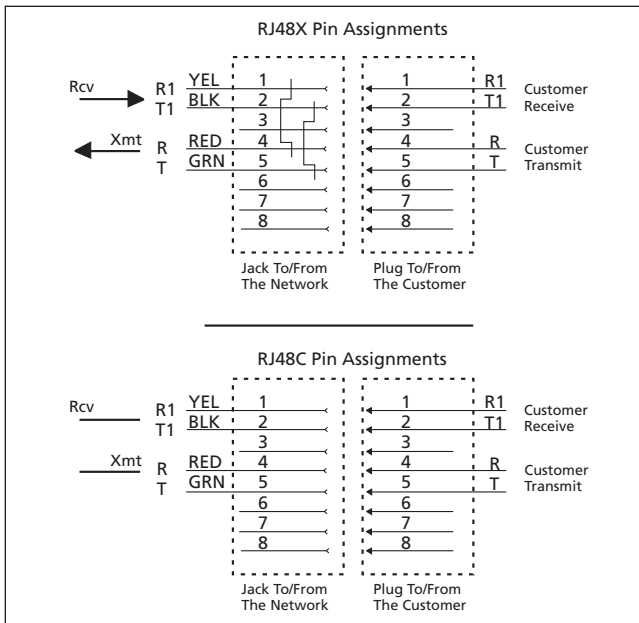


Figure 13: RJ48X and RJ48C Pin Assignment

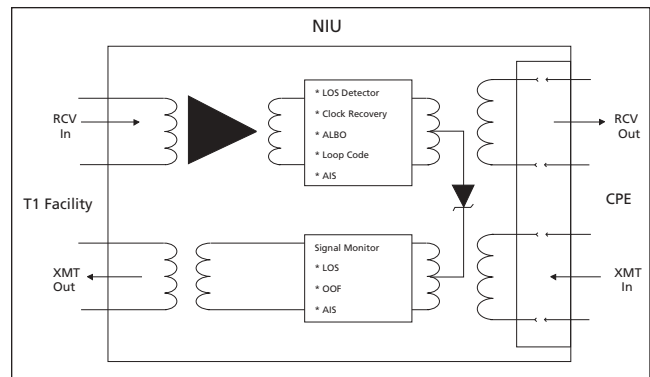


Figure 15: Network Interface Unit (NIU)

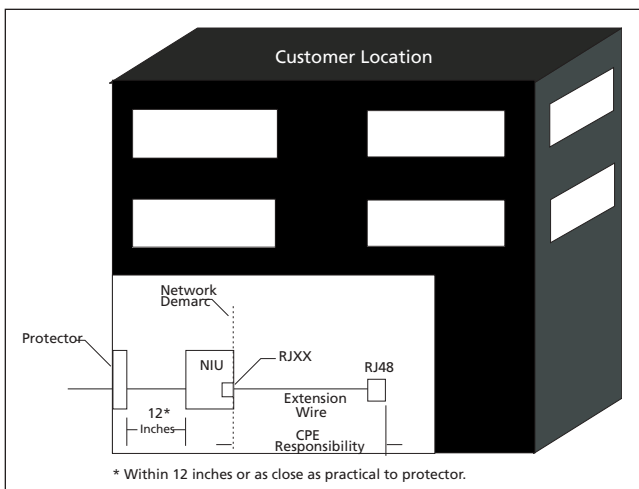


Figure 14: Customer Demarcation Location Selection

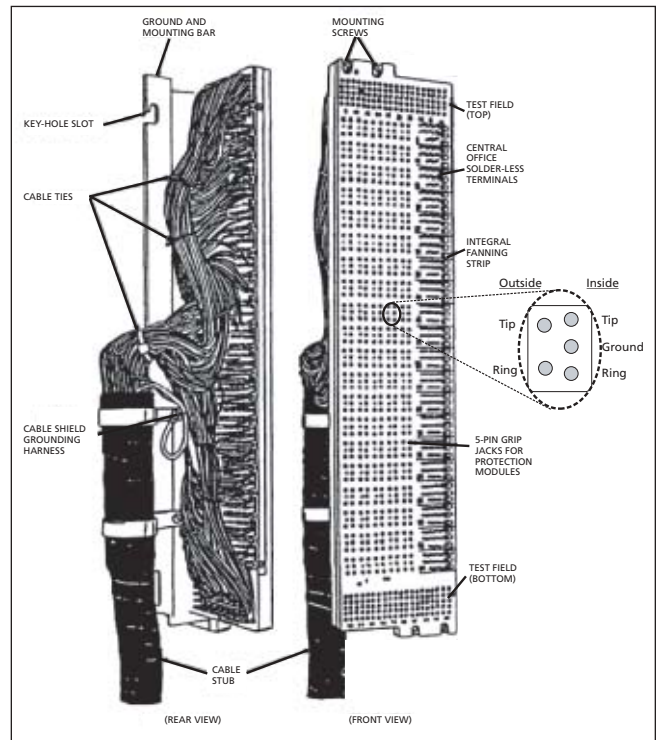


Figure 16: Main Distribution Frame (Type 303)

Table 4: Station Wire Color Codes

Type	Color Code
Two-Pair	1st pair (Tip – Green)
	1st pair (Ring – Red)
	2nd pair (Tip – Black)
	2nd pair (Ring – Yellow)
	OR
	1st pair (Tip – White)
Three-Pair	1st pair (Ring – Blue)
	2nd pair (Tip – White)
	2nd pair (Ring – Orange)
	1st pair (Tip – Green)
	1st pair (Ring – Red)
	2nd pair (Tip – Black)
	2nd pair (Ring – Yellow)
	3rd pair (Tip – White)
	3rd pair (Ring – Blue)
	OR
	1st pair (Tip – White)
	1st pair (Ring – Blue)
2nd pair (Tip – White)	
2nd pair (Ring – Orange)	
3rd pair (Tip – White)	
3rd pair (Ring – Green)	

Network Interface Unit (NIU)

The Network Interface Unit (NIU) serves as the interface between network equipment and customer premise equipment (CPE). It is located at the customer premise, but is provided by the service provider. An NIU is a test access facility for network technicians and provides remote loopback on command. It will also be referred to as a smart jack.

Equipment options for the NIU may vary, depending on the manufacturer. However, most manufacturers follow the same general principles as shown in Table 5.

Main Distribution Frame (MDF)

The Main Distribution Frame:

- Possesses central office (CO) span cable termination capabilities.
- Allows test access and trouble isolation between inside and outside facilities.
- Provides a point for protecting all hi-cap circuits via a protector module:
 - Point-of-surge voltage protection.
 - Solid-state voltage limiting device.
 - 400 volt Tip to Ring (T-R) and 300 volt Tip to Ground (T-Gnd) and Ring Ring to ground (R-Gnd) rating.
 - An isolated device for inside and outside cable and/or equipment.
 - Long pins are the Tip and Ring outside plant conductors (Memory aide: Long = Local Loop).
 - Short pins are the Tip and Ring of the C.O. equipment.
 - Disconnects the C.O. while maintaining protection in the Outside Plant (OSP) when inserted to the indent position (partially in).

Office Repeater

The Office Terminating Repeater (OTR) is located in the Central Office and provides regulated current to power span equipment. The OTR provides simplex current for all the repeaters on the T1 link and regenerates the DS1 signal before routing takes place.

Equipment options vary for the Office Repeater, depending on the manufacturer. Examples are shown in Table 6.

Table 5: Equipment Options for the NIU, SAMPLE

Option	Setting	Description
S1 XMT LBO	OUT (Depends on end-section design)	Transmit Line Buildout (LBO) inserts loss to compensate for a short span between the customer and the adjacent repeater.
S3 Power	—— (Loop) customer.	Unit power option depends on span design: <ul style="list-style-type: none"> ■ Loop = Span-powered NIU with 60 milliamps current looped. ■ Through = Span powered NIU with current passed to the ■ Local = NIU is powered from a local external source.
S5-1 LB/AIS	LB	NIU action upon loss of signal from the customer is either: <ul style="list-style-type: none"> ■ LB = Loopback in both directions. ■ AIS = Send AIS to the network.
S5-2 LOS/DIS	LOS ENABLE	Enables the function selected by S5-1 above.
S5-3 TO/DIS	TO	Set to "TO" to enable the 60 minute auto loopback time-out.
S5-4 REGEN/DIS	——	Enables the regeneration on Side 1 RX path, 0 dBdsx to the customer. If the end section loss is greater than 15 dB, then enable the REGEN for 0 dBdsx to the customer.
S5-5 INBAND/ AUTO	INBAND	Recognizes in-band loopback codes regardless of frame format (Superframe [SF] or Extended Superframe [ESF]).

Table 6: Equipment Options for the OTR, SAMPLE

Option	Setting	Description
SW1 & 2 Trans Pad	0 dB — UP, DN, DN, DN, DN, UP UP	Transmit LBO pad value depends on the end section loss. Normally a 0-dB setting is used. (LBO + Loss = 15 dB maximum)
SW3 CA EQ	1 to 5 = OFF 6 = ON	Set according to the C.O. cable length from the shelf to the DSX panel. Normally set for 0 to 150 ft, except in large offices.
SW4 PWR	C1 = ±130 V	Simplex power feed set for 130 V dc
SW5 ERR SET	A = DN, B = DN, C = DN, D = UP AMI D = DN B8ZS	Error detection options: error threshold is disabled while the line code format is set according to the line code used.
J5 PWR	ON BD	This strap is set according to the power method used for the OTR shelf. In most cases, the shelf is wired for power to be supplied by the OTR card's "on-board" 60 mA power regulator.
J6 RCVR	DIS	Disable the receiver shut down option when the error threshold is exceeded.

Digital Signal Cross-Connect (DSX)

The Digital Signal Cross-Connect jack panels:

- Provide a common point of interconnection of the DS1 facilities through the Central Office by using semi-permanent jumper cross-connects.
 - Two separate jack assignments for each circuit.
 - The OUT jack of the DS1 facility connects to the IN jack of another via the “TN” and “RN” pins on the pin block.
 - Allows labeling of the circuit identification number for cross-connect assignments via a numbered designation strip below the jacks or by using trace cards.
- Are directly cabled to office equipment such as:
 - Line Terminating Shelves (LTSs) for Office Repeaters
 - Fiber multiplex DS1 channels
 - Central Office DS1 digital interface facilities/ports
 - D4 channel Banks or other Mux equipment
- Provide easy DS1 test access to:
 - Non-intrusively monitor circuits through bridge jacks
 - Test circuits (100 ohm termination)
 - Isolate trouble
 - Provide manual loopback via a patch cord
 - Provide service restoration via patching to another facility, if another facility is available
- Provide an LED indicator for cross-connected facilities

- Employ the use of circuit guard plugs (dummy plugs) to protect critical circuits, including:
 - 911 circuits
 - Federal Aviation Administration (FAA) air traffic control
 - Government circuits, civil defense circuits, etc.

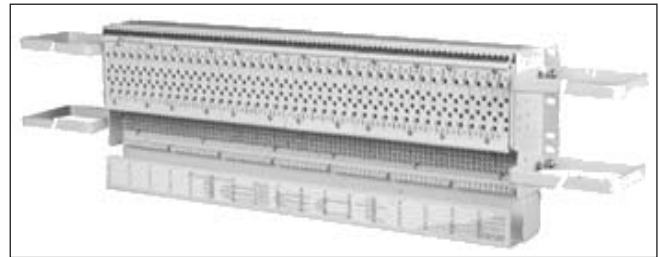


Figure 17: Sample DSX

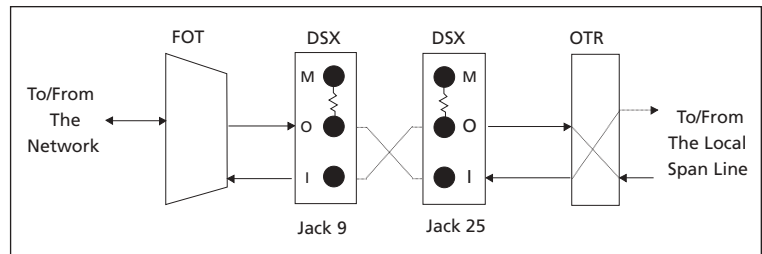


Figure 18: DSX Jack Layout for a Typical Circuit

Table 7: DSX Jack Use/Description

Jack	Purpose	Explanation
MON	<ul style="list-style-type: none"> ■ Is connected to the OUT jack through an isolation resistor ■ Checks circuit quality without interrupting service by monitoring the customer’s live signal ■ Standard signal level is -20 dBdsx (monitor) 	Inserting a plug or cord into the MON jack illuminates both the LED immediately above the jack and above the corresponding cross-connected facility if the Trace Lead (TL) jumper is installed
OUT	<ul style="list-style-type: none"> ■ Is directly cabled to the receive signal of the facility ■ Is the signal coming out of the span, terminal, or switch? ■ Standard signal level is 0 dBdsx, at a 100-ohm termination 	The OUT jack of one DS1 facility is connected to the IN jack of another DS1 facility
IN	<ul style="list-style-type: none"> ■ Is directly cabled to the transmit side of the facility ■ Carries the signal going into the span, terminal, or switches 	The IN jack of one DS1 facility is connected to the OUT jack of another DS1 facility

WARNING: IN and OUT jacks are open-type jacks. In other words, when a plug is inserted into the jack, the signal is interrupted. Plugging into either jack will cause a service interruption to a working circuit.

Testing and Troubleshooting T1 Networks

T1 circuits and network equipment must be properly tested and maintained to perform to maximum efficiency. A basic understanding of signal distortion types is required for proper support.

Performance Parameters

Logic Errors or Bit Errors are the generation or deletion of a one (1) pulse between the transmitted data at one end and the receive data at the other end. Results of bit errors may be observed as:

- Pops in a voice circuit
- An analog modem adjusting to a lower speed
- Data errors and retransmission in a digital circuit, causing reduced throughput.

Bit Error Rate (BER) is the ratio of the number of logic bit errors to the total number of bits transmitted in a given time frame. BER is often expressed in exponents such as those shown in Table 8.

Table 8: Bit Error Rates

Rate	Error per Bits	One Error Every
10^{-3}	1 in 1,000	1.54 seconds
10^{-7}	1 in 10,000,000	6.5 seconds
10^{-8}	1 in 100,000,000	65 seconds
10^{-9}	1 in 1,000,000,000	11 minutes

BER is expressed in terms of $n \times 10^{-9}$, where n is the number of errors over a period of time.

An Errored Second (ES) is any second in which one or more bit errors are received. In the case of Extended Super Frame (ESF), this parameter is a count of one of the following parameters:

- One-second intervals containing one or more Cyclic Redundancy Check six (CRC-6) errors
- One or more controlled slip events
- One or more severely errored framing events that is either out-of-frame or change-of-frame alignment. In the case of superframe, D4, this parameter is a count of one of the following option:
 - One or more controlled slip events
 - One or more severely errored framing events
 - One-second intervals containing one or more Framing bit error events

An Error-Free Second (EFS) is any one-second period in which no error events occur. The proportion of error-free seconds is the ratio of one-second intervals not containing any error events to the total number of seconds in an observed period. This proportion is expressed as a percent of error-free seconds.

A Severely Errored Second is any one-second interval having a BER greater than 10^{-3} . In the case of ESF, it is the count of one of the following options:

- One-second intervals with 320 or more CRC-6 code violations
- A severely errored second event

In the case of superframe, D4, it is a count of one-second intervals with eight or more frame slip events or severely errored framing events.

Availability is the measure of the relative amount of time that a service is "usable" by a customer, presented as a percent over a consecutive 12 month period. T1 service objectives are as follows:

- Acceptance limit is 99.99% over a one year period
 - Out-of-Service limit is BER greater than 10^{-3} in each of 10 consecutive one-second intervals
- Other measures that are tied to availability are:
- Unavailable seconds, which is defined as 10 consecutive seconds with a BER worse than 1×10^{-3}
 - Degraded minutes are minutes in which the BER is between 1×10^{-3} and 1×10^{-6}

A measurement of T1 signal strength in dB relative to a standard 6 volt peak-to-peak ($6 V_{p-p}$) signal is known as dBdsx. The standard measure is 0 dBdsx and is the output of a normal repeater circuit. Correct signal strength at the Digital Cross-Connect (DSX) OUT jack is 0 dBdsx and at the DSX Monitor (MON) jack -20 dBdsx (plus or minus 2 dB).

Table 9: Signal Strength dBdsx to Volts Peak-to-Peak Cross Reference

dBdsx	V_{p-p}	dBdsx	V_{p-p}
+6	11.97	-16	1.00
+3	8.48	-18	0.76
0	6.00	-20	0.60
-3	4.25	-28	0.24
-6	3.01	-30	0.19
-9	2.13		

A slip in a synchronous digital network is the occurrence of digital signal buffer overflow or underflow. Buffers act like reservoirs, filling or draining to accommodate frequency differences or phase variation. As long as the variations do not exceed their capacity, the buffer will operate error-free.

When excess variations occur, buffers may either overflow, deleting blocks of bits, or underflow, repeating a block of bits, resulting in slips. These slips may be classified as either controlled or uncontrolled.

Controlled slip is the overflow or underflow of a T1 frame buffer, resulting in deleting or repeating of one frame, a block of 192 bits, of data. This is often referred to as a frame slip. These frame slips do not affect framing and may be heard as a click on voice circuits. Frame slips do, however, seriously affect digital circuits as data is lost and requires retransmission.

Uncontrolled slip is the overflow or underflow of an unframed buffer, resulting in deleting or repeating a portion of a frame of data. These are much more severe than controlled slips because they result in a framing bit position shift known as a Change of Frame Alignment. Change of Frame Alignment causes an out-of-frame condition in the downstream T1 terminal. This may result in as many as 7,000 bit errors as compared to 192 bit errors in a controlled slip.

Clock slip is a term used to describe the phase variation equal to a single T1 bit time slot or UI of 0.648's. It does not refer to a buffer adding or deleting a bit time, but rather the drifting of a received signal as compared to a reference signal.

Error Insertion is a function available on Digital Signal, Level 1 (DS1) analyzers that allows the operator the ability to transmit a predetermined number of bit errors on the circuit under test. This is not a performance parameter; however, this is useful in verifying that the signal sent is the signal being monitored.

Excess Zeros is a signal containing 16 or more consecutive zeros. Standards require that no more than 15 consecutive zeros be transmitted to maintain ones density for repeater clock circuits.

When an incorrect value appears in the time slot reserved for the framing bit (bit 193) a Frame Error is created. Frame formats follow a predetermined sequence that can easily be monitored by an extended in-service monitor test with a DS1 analyzer.

Stress Patterns

A stress pattern is a predetermined sequence of logical ones and zeros used for T1 installation testing and troubleshooting.

The test routines are called stress patterns because they stress the operating limits of T1 equipment and connecting facilities regarding ones density, consecutive zeros and coding.

Test patterns are standard among test equipment vendors and can be transmitted in the framed or unframed format. The framed format is the recommended standard for network testing. One exception to this rule is the All Ones pattern, which is recommended for maximum stress of a circuit's power. It uses the unframed format.

Alarm and Status Conditions

The Alarm Indication Signal (AIS) is an unframed ALL ONES signal. It is normally transmitted by multiplex or interface equipment upon a loss of signal and will continue for the duration of the service loss. This is also known as a blue alarm.

Network equipment is Out of Frame (OOF) or sync when framing bits are in error in the range of 2-of-5 to 2-of-4.

Loss of Signal/Synchronization (LOS), also referred to as red alarm, exists when the loss of signal on a receiving terminal is for duration of 2.0 to 3.0 seconds.

A yellow alarm is transmitted in the outgoing direction when a terminal recognizes a loss of the receive signal. For example:

- Superframe, D4 – Bit two in every eight-bit time slot will be zero
- Extended Superframe, ESF – Sent in the ESF data link by a 16-bit pattern of eight ones followed by eight zeros

A yellow alarm indicates any of the following conditions:

- Bad transmit Mux
- Bad cable
- Bad receive section at the far end

Cyclic Redundancy Check (CRC) is an extremely accurate way to check for bit errors in transmitted signals in the ESF framing format. All of the data bits in one ESF (24 X 193 = 4632 bits) are considered as one long binary number. This number is divided by another binary number, which is called a constant. The six least significant bits of the remainder are sent as CRC bits during the next ESF.

At the receiving end, the same constant is applied to the 4632-bit ESF and the six least significant bits of the remainder are stored and compared with the CRC bits received during the next ESF. Any difference is flagged as a CRC error.

Test equipment uses the same constant and algorithm to check for errors in the customer's live data, resulting in the best method of in-service monitoring of circuit quality.

Table 10: Stress Patterns and Definitions

Pattern/Test	Description
QRSS	Quasi-Random Sequence Signal (QRSS) which generates every combination of a 20 bit word, repeats every 1,048,575 bits, has 50 percent ones density, and has no excess zeros. QRSS simulates live T1 traffic and is the standard pattern used to measure the T1 BER.
3-IN-24 (AMI)	This pattern contains the longest string of consecutive zeros (15), with the lowest ones density (12.5%). This pattern simultaneously stresses minimum ones density and the maximum number of consecutive zeros. The D4 framed format of 3-IN-24 may cause a D4 yellow alarm for framed circuits, depending on the alignment of one bits to frame. F01000100 0000000000000 100. . .
1:7 or 1-IN-8 (B8ZS)	Only a single one in an eight-bit repeating sequence. This pattern stresses the minimum ones density of 12.5%. It should be used when testing facilities set for Bipolar 8-bit Zero Substitution coding as the 3-IN-24 pattern increases to 29.5% when converted to B8ZS. May cause a D4 yellow alarm for framed circuits. F01000000 01000000 01000000. . .
ALL ONES	This pattern is composed of ones only. The pattern causes the repeater to consume the maximum amount of power. If direct current DC to the repeater is regulated properly, the repeater will have no trouble transmitting the long sequence. This pattern should be used when measuring span power regulation (60 mA, 100 m,. Or 140 mA.).
ALL ZEROS	This pattern is composed of zeros only. It must be encoded with either B8ZS or Zero-Byte Time Slot Interchange (ZBTSI) zero suppression before being transmitted to the network. It is effective in finding equipment misoptioned for Alternate Mark Inversion (AMI), such as fiber/radio multiplex low-speed inputs.
2-IN-8	This pattern contains a maximum of four consecutive zeros. This will not invoke a B8ZS sequence because eight consecutive zeros are required to cause a B8ZS substitution. The pattern is effective in finding equipment misoptioned for B8ZS.
1-IN-16	This pattern is a sequence of a one and 15 zeros in the following form: 0100 0000 0000 0000. The maximum number of sequential zeros is (16) sixteen, when transmitted framed, and 15 when transmitted unframed. This pattern is useful when testing for mis-optioned AMI/B8ZS equipment.
OCT 55 DALY 55	These patterns stress the timing recovery circuits of line cards and the preamplifier/equalizer circuits of repeaters using discrete component ALBOs.
2 ²⁰ -1 2 ¹⁵ -1 2 ²³ -1	These patterns stress circuits beyond specification to determine operating margin. These are optional and should not be used to report network trouble.
63 511 2047 R2047	These patterns are useful for testing low speed data applications. They would be useful in a Fractional T1 Application. For example, DDS, RS232 or RS449.
BTP Bridge Tap Test	The BTP test transmits and receives 22 test patterns of various ones density to locate possible bridge taps located on the DS1 span. The test length is approximately 10 minutes with each pattern tested at 23-second intervals. The test is continuous and will repeat when the test reaches the end. The 22 patterns are listed as follows: ONES 1:1 1:3 1:5 1:6 1:7 2:8 2IN8 2:9 2:10 2:11 2:12 2:13 2:14 3IN18 3IN19 3IN20 3IN21 3IN22 3IN23 3IN24 QRSS
MPT Multi- Pattern Test	The MPT test transmits and receives 5 test patterns. The test length is approximately 15 minutes with each pattern tested at approximately 3-minute intervals. This test is useful for verifying the DS1 spans data carrying integrity. The 5 patterns are listed as follows: ONES 1:7 2IN8 3IN24 QRSS

Common Tests Performed With the 20T1 Test Set

The operating modes are setup via the default menu. The menu that shows the test results is the best way to remember the operating mode menus. Up and down keys are provided under the MODE label for selecting the desired mode.

20T1 Modes of Operation

There are presently 13 operating modes. A brief explanation of each mode is given below:

NORM — T1 Norm Mode. This mode configures all 24 DS0 channels of a DS1 to contain 1 of 18 selectable patterns. The user may also select the desired framing and line code. This mode is typically used for DS1 turn-up and verification. The transmitter is configured like the receiver in the default mode.

AUTO — Automatic T1 Mode. The AUTO mode places the unit into an Auto-evaluation of the incoming DS1 signal. The 20T1 will attempt to find Frame, Pattern and Line Code of the incoming received DS1 signal. When a loss of signal is detected, the unit will automatically enter into an AUTO-evaluate mode.

The Transmitter and Receiver are independent. The receiver is always in the Auto-detect mode looking for Framing, Pattern and Line Code. This mode is considered full 24 channel BERT.

Fx56 — Fractional T1 (Nx56) Mode. This mode allows the user to test in a Fractional DS1 environment. Only 7 bits of data are available in each time slot. The receiver and transmitter are manually configured for frame, pattern and line code via the Default/Results Menu. The Transmit Menu is not available when operating in this Mode. The Channels are configured in the Auxiliary Menu (AUX) Menu.

Fx64 — Fractional T1 (Nx64) Mode. This mode allows the user to test in a Fractional DS1 environment. The full 8-bits of data are available in each time slot. The receiver and transmitter are manually configured for frame, pattern and line code via the Default/Results Menu. The Transmit Menu is not available when operating in this Mode. The Channels are configured in the Auxiliary Menu (AUX) Menu.

D/I — Half Duplex Drop and Insert Mode. This mode allows the user to drop an individual DS0 to the speaker and receive BERT engine. At the same time, either pattern data or a tone may be inserted into the out-going DS0. The other 23 time slots of the DS1 are left undisturbed. The receiver and transmitter are manually configured for frame, pattern and line code via the Default/Results Menu. The drop channel is selected via the CHANNEL select keys on the front panel. The transmit menu selects the desired insertion data channel, whether it is pattern or tone frequency and level.

TONE — Insert Tone Mode. This mode allows the user to insert fixed frequencies of 404 Hz, 1004Hz and 2804Hz, or swept tones from +3 dB to -20 dB. The receiver and transmitter are manually configured for frame, pattern and line code via the default/results menu. The frequency, level and insert channel is selected via the transmit setup menu. The receive DS0 channel drop is independent of the DS0 insertion channel. This is valuable in the sense that the user could listen for crosstalk in adjacent idle channels if desired.

LLB — Local Loop Back or Repeater Mode. This mode loops back the currently received DS1 datastream and is often referred to as a THRU mode. Individual DS0s may be dropped to the speaker and errors may be inserted into the outgoing datastream. The receiver is configured for auto-detect and is passed through to the transmitter undisturbed.

TLB — Test Loop Back or Repeater/CSU Mode. This mode is similar to the LLB mode with one major difference. The receiver will continue to BERT the data as in the LLB mode but the receiver will correct any BPV errors and retime the data before sending it back out the transmitter. Individual DS0s may still be dropped to the speaker and errors may also be inserted into the transmit datastream.

DLAY — Round Trip Loop Delay Measurement Mode. This mode is an out-of-service test that measures the amount of time it takes for a single bit to propagate through the network. The test set must be in pattern sync. By pressing the logic inject key, the test set will insert a single logic error into the DS1 payload. At the same time, a one-millisecond counter is started and the receiver will start looking for the bit error. Once the bit error has been detected, the counter will stop and display the information in the results screen as [LoopDly XXXXXXXX]. The measurement has a one-millisecond resolution.

BTP — Bridge Tap Test Mode. The BTP test mode transmits and receives 22 test patterns of various one's density to locate possible bridge taps located on the DS1 span. The test length is approximately 10 minutes with each pattern tested at 23-second intervals. The test is continuous and will repeat when the test reaches the end. The 22 patterns are listed as follows:

ONES	1:1	1:3	1:5	1:6	1:7
2:8	2IN8	2:9	2:10	2:11	2:12
2:13	2:14	3IN18	3IN19	3IN20	3IN21
3IN22	3IN23	3IN24	QRSS		

MPT — Multi-Pattern Test Mode. The MPT test mode transmits and receives 5 test patterns. The test length is approximately 15 minutes with each pattern tested at approximately 3-minute intervals. This test is useful for verifying the DS1 spans data carrying integrity.

The 5 patterns are listed as follows:

ONES 1:7 2IN8 3IN24 QRSS

CSU — CSU Emulation Mode. When the CSU mode is selected the 20T1 is configured to emulate a Customer Service Unit (CSU). The instrument configuration is as follows:

The line termination is set to TERM (only mode available).

The Tx clock source is set to Rx (only mode available). When configured for the Rx mode, the receiver clock will be used for the transmit clock timing element.

The frame, pattern and line code are manually configured in the default menu.

The Tx LBO is configured in the AUX menu.

When the CSU is in the normal mode and is not looped-up, the transmitter will send either a framed all one's or an unframed all one's depending on the selection of the framing in the default menu.

The 20T1 will respond to either a CSU loop-up/down code or a payload loop-up/down code. If a CSU or payload loop-up code has been detected, the 20T1 will give an audible indication and illuminate the received loop up LED for 3 seconds and display <<CSU or PAYLD LOOPED UP>> on line 3 of the LCD. The Tx LBO will be set to a 0 dB (6 Vp-p) DSX level. If a CSU or payload loop-down has been detected, the 20T1 will light the received loop down LED for three seconds and display <<CSU NORM MODE>> on line 3 of the LCD. The Tx LBO will return to user selection as defined in the AUX menu.

When the CSU is looped-up, the 20T1 can do a non-intrusive BERT on the incoming data. T1 performance monitoring is still performed even if pattern sync is not achieved.

NIU — NIU Emulation Mode. When the operator selects the NIU mode, the unit is configured to emulate a NIU (Network Interface Unit). The InterroGatr20T1 is configured as follows:

The line termination is forced to TERM (only mode available).

The Tx clock source is forced to Rx (only mode available). When configured for the Rx mode, the receive clock will be used for the transmit clock timing element.

The receive frame, pattern and line code are manually configured in the default menu. The transmitter will always configure itself from the frame, pattern and line code settings of the receiver.

When the NIU is in the normal mode and is not looped-up, the transmitter will send the frame, pattern and line code that was configured in the default menu toward the CO. At the same time, the receiver is doing a BERT on the incoming data from the CO. This is effectively the same as being in the Fx64 - Fractional T1 mode with all channels enabled.

When the InterroGatr20T1 is looped-up, the receiver will do a non-intrusive BERT on the incoming data. T1 performance monitoring is still performed even if pattern sync is not achieved. The receive data is passed to the transmitter unchanged with timing being derived from the CO.

The receiver will respond to an NIU5 loop-up/down code. If an NIU5 loop-up code has been detected, the InterroGatr20T1 will give an audible indication and illuminate the receive loop up LED for three seconds and display << NIU LOOPED UP >> on line 3 of the LCD.

If an NIU loop-down has been detected, the InterroGatr20T1 will light the receive loop down LED for three seconds and display << NIU NORM MODE >> on line 3 of the LCD.

Performing Automatic Evaluation

When the mode is configured for AUTO, LLB or TLB and the user inserts a bantam-ended test cord into the RX jack of the 20T1, the test set will automatically evaluate the incoming signal and determine its framing type and BERT patterns. The 20T1 first determines the frame type that is currently being used on the line (D4, ESF, SLC96, or NONE). Then, it determines the pattern that is being transmitted on the line. If the 20T1 is unable to detect one of the BERT patterns supported by the 20T1, or if live traffic is present, then the unit will display LIVE above the PATTERN label on line 4 of the LCD display signifying that a pattern could not be found. Subsequent presses of the RESTART key will start a new evaluate.

The 20T1 only performs automatic evaluation of the incoming signal if there is a valid input signal present at the RX jack of the 20T1. If the input signal disappears during the cycle, the 20T1 will stop its evaluation until the signal is reapplied.

In this mode, the receiver and transmitter of the 20T1 are totally independent. Therefore, the evaluated Rx signal and the receiver setup do not affect the transmitter. The transmitter is independently configured in the Transmitter Setup Menu.

Monitoring Live Traffic

Use the following procedures to monitor live traffic.

1. Select a monitor point at which to perform your evaluation. The monitor point may be “monitor” jacks on a CSU, NIU, or DSX jack field, or the 20T1 may be “bridged” across one side of the T1 line at any electrical access point.
2. Use the MODE up and down arrow keys and select the AUTO (Automatic) Mode. This mode places the transmitter and receiver in full 24-channel BERT mode. The receiver is always in auto-detect mode and is looking for frame and line code. Subsequent presses of the RESTART key will initiate a pattern search and if one is not found, LIVE pattern data will be declared. The Transmitter is independent and may be configured via the Transmitter Setup Menu.
3. Use the TERMINATION switch on the front panel of the 20T1 to select BRDG or MON. Select MON if the chosen test point is provided with the 432-ohm isolation resistors to isolate the test set from the T1 line (such as a DSX monitor jack in a central office). Select BRDG if the test set is to be bridged across the T1 line (such as at a 66 block).
4. Insert a bantam-ended test cord into the Rx T1 receiver of the 20T1.
5. Connect the other end of the test cord to the selected access point.

Note: Not all CSU manufacturers provide proper isolation from the monitor jacks to the T1 line. To determine the proper setting for your 20T1, refer to the literature provided to you by your CSU manufacturer.

6. Press the RESTART key to erase any errors registered during the setup.
7. Observe the 20T1 indicators.

Status LEDs — These LEDs provide information about the health of the T1 signal.

Frame Sync LED — This LED indicates the frame pattern of the incoming signal: D4, ESF, or SLC96. If the 20T1 does not detect a frame pattern, the FRAME SYNC LED will not illuminate. No frame is a legitimate condition if the incoming signal is unframed.

Line Code LEDs — These LEDs (AMI and B8ZS) indicate the detected line coding.

Test Summary LED — The 20T1 detects BPV and FRAME errors on any T1 signal (if frame sync is established). CRC errors are recorded on ESF- framed signals. If an error is detected, the TEST SUMMARY LED will illuminate. Use the display arrow keys to select SUMRY. This will put the top two lines of the display in the display summary mode. Use the RESULTS arrow keys to view the error type and observe the number of recorded errors on the 20T1 front-panel display.

8. If necessary, perform additional analysis of the T1 signal.

DS1 Frequency — To observe the frequency of the DS1 signal (in Hz), press the RESULTS arrow keys until the DS1 FREQ parameter is observed on the display.

DS1 Level — To observe the level of the DS1 signal (in dBdsx or volts), press the RESULTS arrow keys until the Rx1levl parameter is observed on the display.

Note: When readings are taken from a DSX monitor jack with the TERMINATION switch set to DSX- MON, the isolation resistors will cause the level reading to be approximately -20 dB below the actual line level. To determine the actual line level from a DSX monitor jack, 20 dB must be added to the reading shown on the 20T1 display (if the readings are in dBdsx). If the readings have been converted to Vp-p, multiply them by 10 in order to get a true line-level measurement.

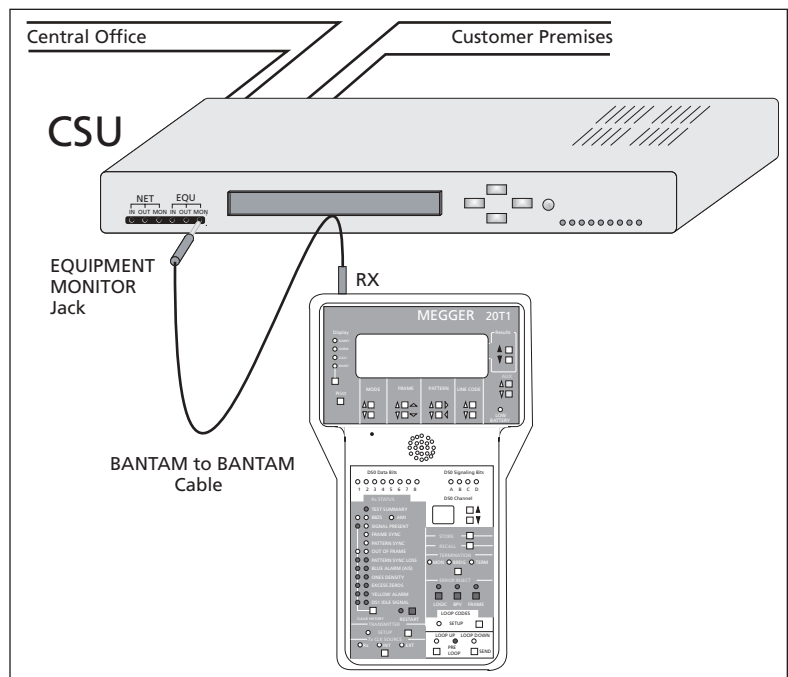


Figure 19: Evaluating Live Traffic

9. To observe parameters associated with specific DS0s, proceed with the following steps.
 - Use the yellow AUX menus up and down arrow keys to select the SIGNALING TYPE auxiliary menu. Utilize the yellow coded arrow keys to select the signaling type used on the T1 facility: ROBBED BIT or Common Channel Signaling (CCIS). The selected signaling type will blink to indicate your choice.
 - Use the CHANNEL arrow keys to select the DS0 to be monitored.
10. Observe the signaling bits of the selected DS0. A and B signaling bits will be displayed for D4 or SLC96 framed signals. A, B, C, and D signaling bits will be displayed for ESF framed signals.
11. Observe the data bits LEDs, which indicate the 1 or 0 state of the data bits associated with the selected DS0.
12. You can monitor the demodulated audio signal (from the selected DS0) through the speaker. The volume can be adjusted using the volume control.
13. Record the frequency and level of a test tone present on the selected DS0.
 - Use the RESULTS arrow keys to select the DS0 FREQ LED and view the frequency of the test signal (in Hz).
 - Use the RESULTS arrow keys to select the DS0 LEVEL LED and view the level of the test tone in dBm.

Performing a BERT (Bit Error Rate Test)

To perform a Bit Error Rate Test, the T1 circuit must be placed out of service. The object of the test is to determine the Bit Error Rate sustained over a period of time by a test pattern sent over a T1 transmission network. This is accomplished by letting the T1 receiver compare on a bit-by-bit basis, the received/monitored bit stream with a copy of the stream sent by the signal source. In this manner, the T1 receiver can identify any bit errors introduced by the transmission system. The Bit Error Rate is obtained by dividing the Bit Error count by the total number of bits transmitted during the test. The total number of bits is given by 1,544,000 bits times the number of seconds in the test period.

BERT can be performed with a single 20T1 by looping the far end circuit element. While this requires only one person (and one instrument), both transmission directions are tested simultaneously. Consequently, if a problem is observed, additional test sets are required to determine which of the two directions is impaired. The far end can be looped with a patch cord between the XMT and RCV pairs or, more conveniently, by a controllable looping device (CSU, NIU, HDSL circuit element). Figure 20 illustrates the test set up using a single BER test set.

Alternatively, BERT is conveniently performed on an end-to-end basis using two compatible test sets. Both transmission directions are also tested simultaneously, but this time each direction is tested separately. The user can readily determine which transmission direction is impaired. Figure 21 illustrates the test setup using two BER test sets.

Whether one or two sets test sets are used, the basic testing process is the same. The main difference is that when a single test set is used, looping at the far end must precede the start of the BER test proper. If the looping is performed by a circuit element, the loop up code can be supplied by the 20T1.

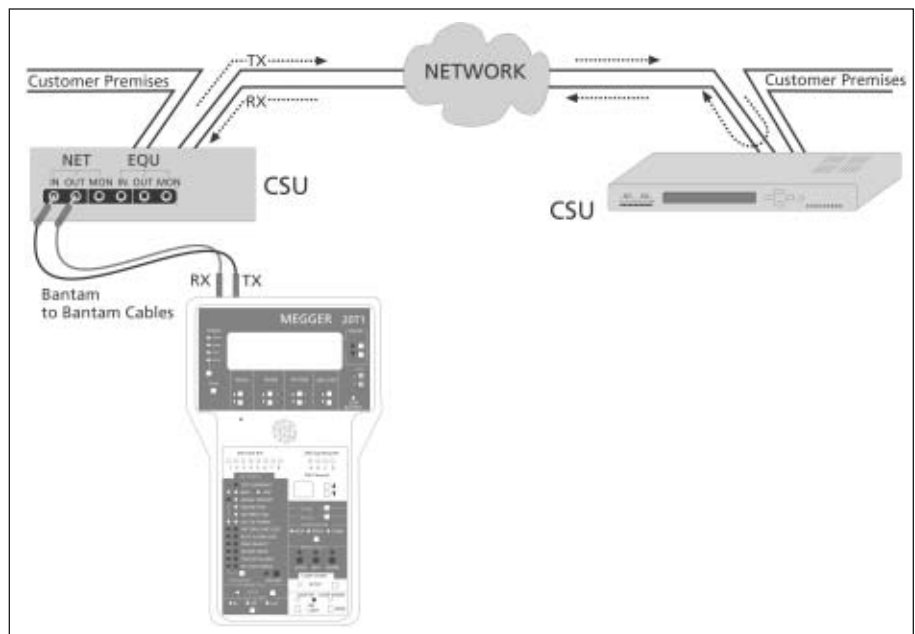


Figure 20: Performing an Out-of-Service BERT

Each test set must be set up as follow:

- Power up the test set.
- Set the receiver termination switch to TERM.
- Select INT for the Tx Clk Source.
- Place the unit in AUTO (automatic mode). Press the transmit setup key and configure the transmit framing, pattern and line code. Patch the Rx input jack to the OUT jack.
- Patch the Tx output jack to the IN jack.
- Press the RESTART key.

As soon as the test pattern received by the T1 Rx is identified, Bit Errors, if any, are detected and counted. The BER can then be readily calculated as noted in the introduction of this procedure.

Performing Clock-Slip Measurements

In order to ensure proper network performance, clocks between various circuit elements must be synchronized. Clock-synchronization problems are a common occurrence when customer premises equipment (CPE), such as PABXs and multiplexers are connected to the public network. The 20T1 has the ability to determine synchronization by measuring the clock-slip count between two clock sources.

To perform a clock-slip measurement, proceed with the following steps.

1. Determine the test measurement points. A clock differential may be made between any two T1 clocking sources. In this example, the network clock is compared to the clock that is recovered from the DS1 signal transmitted from the customer side of the CSU.
2. Insert a bantam-ended test cord into the 20T1 Rx T1 receiver.
3. Use the RECEIVER TERMINATION switch to select MON.
4. Connect the other end of the test cord to the line-side monitor jack of the CSU.

5. Insert a second bantam-ended test cord into the 20T1 REF T1 receiver. If no REF T1 is available, the internal T1 clock source may be used.
6. Connect the other end of the second test cord to the equipment-side monitor jack of the CSU.
7. Press the RESTART key to clear any errors or false indications caused by establishing the connection.
8. Roll the RESULTS scroll keys until the ClkSlps parameter shows up on the LCD Display.

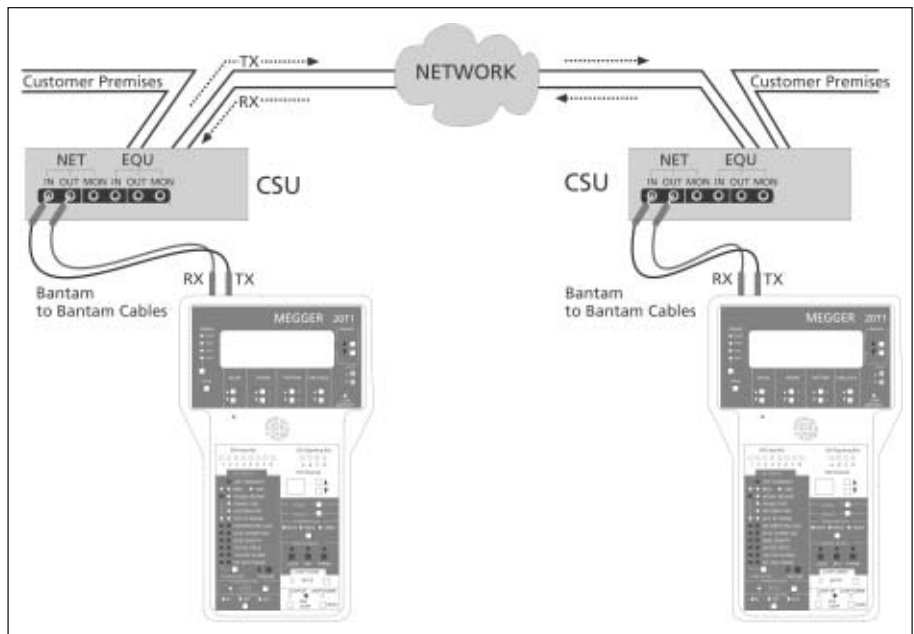


Figure 21: Performing an End-to-End, Out-of-Service BERT

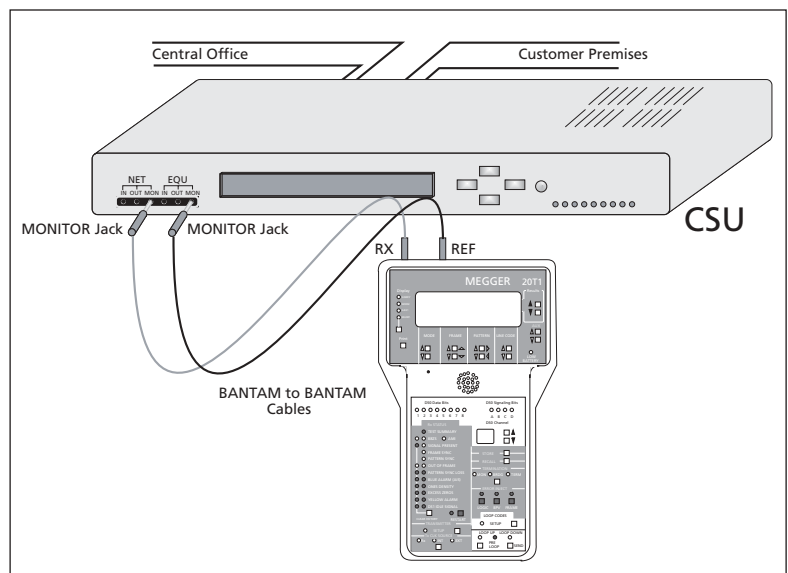


Figure 22: Performing Clock-Slip Measurements

9. Observe the displayed clock-slip count.

The cables may be reversed for this test. If clock slips do occur, the sign (+/-) will be reversed.

During a clock-slip test, other indications are valid for the side of the T1 line connected to the Rx T1 receiver.

Performing a Half Duplex Drop & Insert

Drop & Insert is a method of accessing a live T1 circuit to test an individual DS0 without disturbing the possibly active 23 DS0s. In some cases, the T1 circuit is already turned up and carrying live traffic, but no direct DS0 channel access exists to troubleshoot channel problems. Rather than turn down the complete T1 circuit, Drop & Insert provides an ideal test option.

The Drop & Insert mode can be used for substituting the content of either a single DS0 or a set of channels as in the case of Fractional T1.

The 20T1 offers DS0 circuit testing capabilities, including voice (frequency, level measurement) and the ability to insert three different tones at a variety of levels from -20 dB to +3 dB, a three-tone sweep or a selection of BERT patterns including two user selectable patterns.

Before attempting Drop & Insert testing, it is important to fully understand the complete test set up. Improper patch cord configuration can interrupt the T1 Circuit and, therefore drop all 24 DS0s.

The test is set up as follows:

- With no patch cords attached, set the MODE on the test set to DI.
- Connect a patch cord to the Rx jack and another to the Tx jack on the test set.
- Simultaneously and quickly patch the Rx jack input to the T1 DSX Output and the Tx jack to the DSX Input.

The last step involves breaking the circuit briefly so it must be done quickly and correctly. Done correctly, customer traffic should not be dropped.

The 20T1 is now directly in the T1 circuit and passing all traffic through. By pressing the transmitter setup key, the user can choose either a BERT pattern or TONE for the data content, the desired transmit channel and the

desired pattern or test tone. Press the transmitter setup key again to exit. Roll the PATTERN scroll key from IDLE to INSERT. This will start inserting the selection made in the Transmitter Setup menu whether it is pattern data or a test tone into the selected DS0. Scroll the PATTERN key again to IDLE the selected insertion channel. The test set will insert (7FH) idle code in the selected Transmit channel.

Performing a Loop Delay Measurement on a T1 Circuit

To perform a Loop Delay Measurement, the T1 circuit must be placed out of service. The object of this test is to determine the length of time it takes for one bit of information to propagate through the network and return to the origination point. Therefore the loop must toll grade quality and error free.

The test is performed with a single by looping the Far end circuit element. Figure 23 illustrates the test set up using a single test set.

The user will scroll the MODE keys to DLAY, the Delay Measurement Mode. The test set will transmit ALL ONE's and gain pattern sync. By pressing the logic inject key, the test set will insert a single logic error into the DS1 payload. At the same time, a one-millisecond counter is started and the receiver will start looking for the bit error. Once the bit error has been detected, the counter will stop and display the information in the results screen as [LoopDly XXXXXXXX]. The measurement has 1-millisecond of resolution.

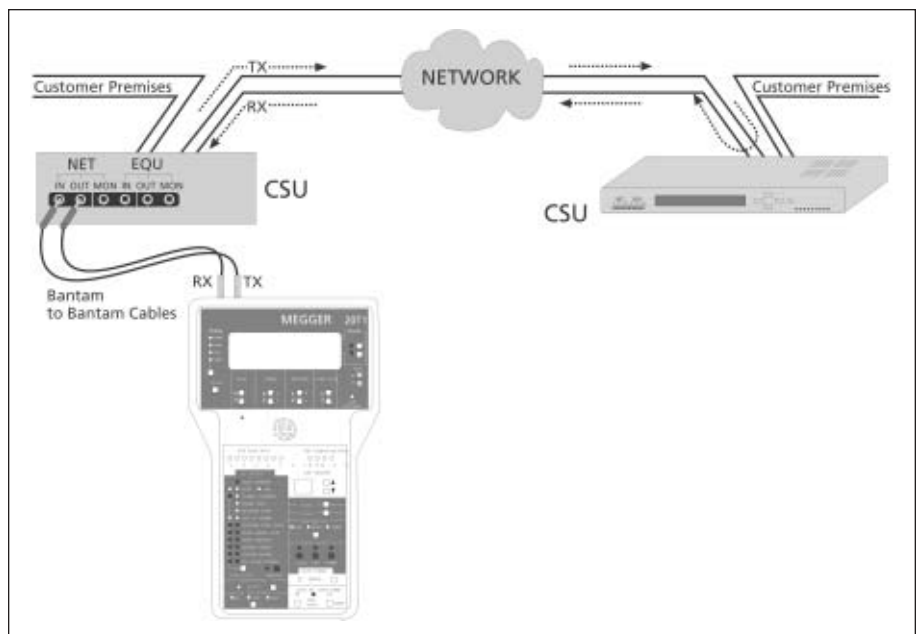


Figure 23: Loop Delay Measurement

The test set is setup as follows:

- Power up the test set.
- Set the receiver Termination switch to TERM.
- Select INT for the Tx Clk Source.
- Place the unit in DLAY (Delay Measurement Mode).
- Configure the test set for Framing and Line Code. The transmitter in this mode is configured like the receiver.
- Patch the Rx input jack to the OUT jack
- Patch the Tx output jack to the IN jack.
- Press the RESTART key.
- Press and release the LOGIC inject key.
- Record the measurement. Pressing the LOGIC inject key will start a new measurement.

Performing a Bridge Tap (BTP) or Multi-pattern (MPT) Test on a T1 Circuit

To perform a BTP or MPT test, the T1 circuit must be placed out of service. The objective of this test is to cycle through fixed length patterns for a fixed duration and record the results. The test is performed with a single InterroGatr 20T1 by looping the far end circuit element. Figure 23 on the previous page illustrates the test set up using a single test set.

BTP

The BTP test mode transmits and receives 22 test patterns of various one's density to locate possible bridge taps located on the DS1 span under test. The test length is approximately 10 minutes with each pattern tested at 23-second intervals. The test is continuous and will repeat when the test reaches the end.

The 22 patterns are listed as follows:

ONES	1:1	1:3	1:5	1:6	1:7
2:8	2IN8	2:9	2:10	2:11	2:12
2:13	2:14	3IN18	3IN19	3IN20	3IN21
3IN22	3IN23	3IN24	QRSS		

The test set is setup as follows:

- Power up the test set.
- Set the receiver termination switch to TERM.
- Select INT for the Tx Clk source.
- Scroll the MODE keys and place the unit in BTP, bridge tap test mode. Configure the test set for framing and line code. The transmitter in this mode is configured like the receiver.

- Patch the Rx input jack to the OUT jack
- Patch the Tx output jack to the IN jack.
- Change the Display Mode key to SUMRY.
- Press the RESTART key.

If the test summary LED is on, this indicates that a test pattern failed or the test set uncovered another anomaly, i.e., frame error, BPV error, frequency deviation and one's density. Scrolling the results keys will indicate the errors discovered while the test was running. If the test fails on a pattern, the user can configure the user patterns to stress only the test pattern(s) that failed.

MPT

The MPT test mode transmits and receives five test patterns. The test length is approximately 15 minutes with each pattern tested at three-minute intervals. The test is continuous and will repeat when the test reaches the end. This test is useful for verifying the DS1 spans data carrying integrity. The (5) patterns are listed as follows:

ONES	1:7	2IN8	3IN24	QRSS
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The test set is setup as follows:

- Power up the test set.
- Set the receiver Termination switch to TERM.
- Select INT for the Tx Clk source.
- Scroll the MODE keys and place the unit in MPT, Multi-Pattern Test, mode. Configure the test set for framing and line code. The transmitter in this mode is configured like the receiver.
- Patch the Rx input jack to the OUT jack
- Patch the Tx output jack to the IN jack.
- Change the Display mode key to SUMRY.
- Press the RESTART key.

If the test summary LED is ON, this indicates that one or more test patterns failed, or the test set uncovered another anomaly, i.e., frame error, BPV error, frequency deviation and one's density. Scrolling the results keys will indicate errors discovered while the test was running. If the test fails on a pattern, the user can configure the user patterns to stress only the pattern(s) that failed.

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